PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 09/933,468 Applicant : Christopher S. MacLellan Filed : August 20, 2001 T.C./A.U. : 2138 Examiner : John J. Tabone, Jr. Docket No. : EMC-01-018 Customer No. : 24227	Confirmation No.: 5620

Certificate of Mailing or Transmission 37 C.F.R. § 1.8
I hereby certify that this correspondence is being transmitted by facsimile on the date shown below to the Patent and Trademark Office at 571-273-8300.
Typed or printed name of person signing this Certificate:
Linda Valanzola *6/12/06*   *[signature]* *Date*   *Signature*

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

DECLARATION UNDER 37 C.F.R. §1.131

1.   I, Christopher S. MacLellan, am the inventor of the above-referenced U.S. Patent Application No. 09/933,468 entitled "Testing System and Method of Using Same."

2.   Prior to September 14, 2000, I conceived of, and reduced to practice, the invention described and claimed in U. S. Patent Application No. 09/933,468, as evidenced by source code, a portion of which being attached hereto as Exhibit A. The code was created on or before September 14, 2000 as is evidenced by the time stamp at the top of the file of the Exhibit indicating that the file A20SVC.v was last modified on September 14, 2000.

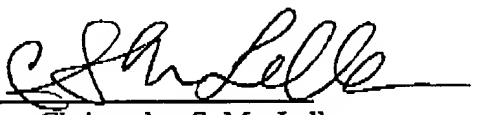Application No. 09/933,468   Docket No. EMC-01-018

Since this is the assignee's proprietary source code, only a portion of the code is included in the Exhibit. The code in its entirety comprises the third logic section recited in the claims.

Exhibit B is an email dated March 20, 2001 in which an invention disclosure conference is scheduled. One of the invention disclosures to be discussed at that conference is the invention described in this U. S. Patent Application No. 09/933,468, i.e., Docket No. EMC-01-018. This invention disclosure is attached as Exhibit C. I note that, although the "Date of Idea (or first disclosure either or written to others)" indicates a date of 11/15/01, this is a typographical error. The intended date was 11/15/2000, which was the date that I first disclosed the invention to others. The typographical error should be obvious, given that the invention disclosure conference was scheduled in March 2001 and the patent application was filed in August 2001.

3.   All of the statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true. These statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application and any patent issuing thereon.

        6-12-2006   By: _____
        Date of Signature   Christopher S. MacLellan

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```
> ls -lat A20SVC.v
-rw-r--r--  1 chrismac symmem     101745 Sep 14  2000 A20SVC.v
> cat A20SVC.v
/* A20 Service Processor */

module A20SVC(CLOCK,
             RESET,
             SRESET,
             MID,

            // UI A Interface
            REQA,       // 0 = Request
            GNTA,       // 0 = Request grant
            TAGA,       // 18-bit TAG field from UI
            CMDA,       // 18-bit COMMAND field from UI
            AD2A,       // 18-bit ADDRESS 2 field from UI
            AD1A,       // 18-bit ADDRESS 1 field from UI
            AD0A,       // 18-bit ADDRESS 0 field from UI
            SDIA,       // 18-bit service data from UI
            SDOA,       // 18-bit service data to UI
            SDCRC1A,    // 18-bit Service data CRC high from UI
            SDCRC0A,    // 18-bit Service data CRC low from UI
            SDONEA,     // 1 = Service Done to UI
            SDRA,       // 1 = Service Data request to UI
            SDVA,       // 1 = Service Data valid to UI
            SERRA,      // 1 = Service Error to UI
            SCRCEA,     // 1 = Service Data CRC Error to UI
            INTERRA,    // 1 = Internal Error to UI
            NOCYCA,     // 1 = No Cycle Indication from UI
            CYCDONEA,   // 1 = Cycle Done Indication from UI
            AW,         // 1 = UI connected with W port
            AX,         // 1 = UI connected with X port
            AY,         // 1 = UI connected with Y port
            AZ,         // 1 = UI connected with Z port
            UTMOVALA,   // 14-bit Upper Timeout Value to UI
            DIAGA,      // 46-bit Diagnostic mode register to UI
            STATA,      // 64-bit Error/Event conduit from UI

            // UI B Interface
            REQB,       // 0 = Request
            GNTB,       // 0 = Request grant
            TAGB,       // 18-bit TAG field from UI
            CMDB,       // 18-bit COMMAND field from UI
            AD2B,       // 18-bit ADDRESS 2 field from UI
            AD1B,       // 18-bit ADDRESS 1 field from UI
            AD0B,       // 18-bit ADDRESS 0 field from UI
            SDIB,       // 18-bit service data from UI
            SDOB,       // 18-bit service data to UI
            SDCRC1B,    // 18-bit Service data CRC high from UI
            SDCRC0B,    // 18-bit Service data CRC low from UI
            SDONEB,     // 1 = Service Done to UI
            SDRB,       // 1 = Service Data request to UI
            SDVB,       // 1 = Service Data valid to UI
            SERRB,      // 1 = Service Error to UI
            SCRCEB,     // 1 = Service Data CRC Error to UI
            INTERRB,    // 1 = Internal Error to UI
            NOCYCB,     // 1 = No Cycle Indication from UI
```

```
                    CYCDONEB,  // 1 = Cycle Done Indication from UI
                    BW,        // 1 = UI connected with W port
                    BX,        // 1 = UI connected with X port
                    BY,        // 1 = UI connected with Y port
                    BZ,        // 1 = UI connected with Z port
                    UTMOVALB,  // 14-bit Upper Timeout Value to UI
                    DIAGB,     // 46-bit Diagnostic mode register to UI
                    STATB,     // 64-bit Error/Event conduit from UI

                    // UI C Interface
                    REQC,      // 0 = Request
                    GNTC,      // 0 = Request grant
                    TAGC,      // 18-bit TAG field from UI
                    CMDC,      // 18-bit COMMAND field from UI
                    AD2C,      // 18-bit ADDRESS 2 field from UI
                    AD1C,      // 18-bit ADDRESS 1 field from UI
                    AD0C,      // 18-bit ADDRESS 0 field from UI
                    SDIC,      // 18-bit service data from UI
                    SDOC,      // 18-bit service data to UI
                    SDONEC,    // 1 = Service Done to UI
                    SDCRC1C,   // 18-bit Service data CRC high from UI
                    SDCRC0C,   // 18-bit Service data CRC low from UI
                    SDRC,      // 1 = Service Data request to UI
                    SDVC,      // 1 = Service Data valid to UI
                    SERRC,     // 1 = Service Error to UI
                    SCRCEC,    // 1 = Service Data CRC Error to UI
                    INTERRC,   // 1 = Internal Error to UI
                    NOCYCC,    // 1 = No Cycle Indication from UI
                    CYCDONEC,  // 1 = Cycle Done Indication from UI
                    CW,        // 1 = UI connected with W port
                    CX,        // 1 = UI connected with X port
                    CY,        // 1 = UI connected with Y port
                    CZ,        // 1 = UI connected with Z port
                    UTMOVALC,  // 14-bit Upper Timeout Value to UI
                    DIAGC,     // 46-bit Diagnostic mode register to UI
                    STATC,     // 64-bit Error/Event conduit from UI

                    // UI D Interface
                    REQD,      // 0 = Request
                    GNTD,      // 0 = Request grant
                    TAGD,      // 18-bit TAG field from UI
                    CMDD,      // 18-bit COMMAND field from UI
                    AD2D,      // 18-bit ADDRESS 2 field from UI
                    AD1D,      // 18-bit ADDRESS 1 field from UI
                    AD0D,      // 18-bit ADDRESS 0 field from UI
                    SDID,      // 18-bit service data from UI
                    SDOD,      // 18-bit service data to UI
                    SDCRC1D,   // 18-bit Service data CRC high from UI
                    SDCRC0D,   // 18-bit Service data CRC low from UI
                    SDONED,    // 1 = Service Done to UI
                    SDRD,      // 1 = Service Data request to UI
                    SDVD,      // 1 = Service Data valid to UI
                    SERRD,     // 1 = Service Error to UI
                    SCRCED,    // 1 = Service Data CRC Error to UI
                    INTERRD,   // 1 = Internal Error to UI
                    NOCYCD,    // 1 = No Cycle Indication from UI
                    CYCDONED,  // 1 = Cycle Done Indication from UI
```

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Mazzarella, Julie

From:	Mazzarella, Julie
Sent:	Tuesday, March 20, 2001 11:27 AM
To:	walton, john (BMC Eng); maclellan, chris; bermingham, mike; Gupta, Krish; Gagne, Christopher
Subject:	Disclosure Conference April 9, 10a.m.-12p.m., Conf. Rm. 21-28 (171 South St.)

Gentlemen,

You will be meeting on Monday, April 9, from 10 a.m. to 12 p.m. in Confrerence Room 21-28 at 171 South Street to discuss the following new invention disclosures:

1. ████████████████████████████

2. ████████████████████████████

3. *System and Method for Reliably Testing Embedded Memory* by Chris MacLellan (EMC-01-018).

Thanks,

Julie Mazzarella
Patent Administrator
Office of the General Counsel
EMC Corporation
35 Parkwood Drive
Hopkinton, MA 01748

BEST AVAILABLE COPY

EMC-01-018

INVENTION RECORD/DISCLOSURE

1. **Title:** System and Method for Reliably Testing Embedded Memory

2. **Description and purpose of the Invention (include drawings, memos, or other explanatory material:** When embedding memory structures (such as SRAM) into a custom design (such as an ASIC), testing the memory during manufacture of the chip is important. This system provides a way to test the memory, not only during chip manufacture, but also at any time during board test and system test. This system also provides a way to inject a fault into the memory to test the test circuit itself. There is protection built into the system which add to the reliability of the design.

3. **Former approaches and disadvantages:** Prior approaches either required a lot of manual test vector generation, additional chip pins dedicated to the memory test circuit, or both. They also took away from the reliability of the design.

4. **Advantages of Invention over former approaches:** This system does not require additional pins or manual test vectors. It also has built-in protection against inadvertent test circuit interference with system operation.

5. **Inventors:** Christopher S. MacLellan

6. **Date of Idea (or first disclosure either oral or written to others):** 11/15/01